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DATE MAILED: 06/23/2005

APPLICATION NO.	APPLICATION NO. FILING DATE FIR		ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/707,844	7,844 11/08/2000 Hidetosh		0819-448	9493	
22204	4 7590 06/23/2005		EXAMINER FARAHANI, DANA		
NIXON PEABODY, LLP 401 9TH STREET, NW					
SUITE 900	CEI, IV VV		ART UNIT	PAPER NUMBER	
WASHINGTON, DC 20004-2128			2891		

Please find below and/or attached an Office communication concerning this application or proceeding.

		Applicatio	n No.	Applicant(s)					
Office Action Summary		09/707,844	4	ISHIDA ET AL.	(m)				
		Examiner		Art Unit	# .				
		Dana Fara	hani	2891					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address									
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).									
Status									
2a)□	Responsive to communication(s) filed on <u>06 June 2005</u> . This action is FINAL. 2b) This action is non-final. Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.								
Dispositi	on of Claims								
 4) Claim(s) 1,2 and 4-10 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) is/are allowed. 6) Claim(s) 1,2 and 4-10 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or election requirement. 									
Applicat	ion Papers								
9) The specification is objected to by the Examiner. 10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.									
Priority (ınder 35 U.S.C. § 119								
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 									
2) Notice No	ot(s) ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449 or PTO/SB/08 er No(s)/Mail Date	8)	4) Interview Summar Paper No(s)/Mail D 5) Notice of Informal 6) Other:	Date)-152)				

Application/Control Number: 09/707,844

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
- 2. Claims 1, 4, 6, and 8-10 are rejected under 35 U.S.C. 102(a) as being anticipated by the Japanese patent application 01-305125, publication No. 03-165058, hereinafter the Japanese reference, which is cited in the Information Disclosure Statement submitted by applicant(s) on 6/06/2005.

Regarding claims 1 and 9, The Japanese reference discloses in figures 4 and 5, a semiconductor device comprising:

a semiconductor substrate 1;

two adjacent semiconductor elements 4 and 6 provided on the principal surface of the substrate;

multiple through holes 3, which pass from the principal surface through the backside of the substrate and are provided in a region of the substrate sandwiched by the two adjacent semiconductor elements so as to substantially eliminate the electrical interference between the two adjacent semiconductor elements; and

a conductor film formed directly on the side faces of the through holes (see the paragraph titled CONSTITUTION below the abstract).

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Regarding claims 4 and 10, a ground wiring layer 12 is on the backside of the substrate connected to the conductor of the through holes 3.

Regarding claim 6, the Japanese reference discloses a semiconductor substrate 1; at least two semiconductor elements 4 and 6 provided on the principal surface of the substrate;

electrodes of the at least two elements provided on the substrate;

a first group of through holes 3, which pass from the principal surface through the backside of the substrate and are provided in respective regions of the substrate under the electrodes;

a first conductor film provided on the side faces of the first group of through holes (see CONSTITUTION);

a second group of through holes 3 (at the right side of the first group of through holes 3, in figure 4), which pass from the principal surface through the backside of the substrate and are provided in a region of the substrate between the elements;

a second conductor film provided on the side faces of the second group of through holes; and

a wiring layer 12, which is provided on the backside of the substrate and is in contact with the first and second conductor films;

wherein the second groups of through holes are provided in different locations from the first group of through holes (figure 4).

Regarding claim 8, the multiple through holes stand in a line (see figure 4).

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 2, 5 and 7 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over the Japanese reference.

Regarding claim 2, the Japanese reference discloses the claimed invention, but does not expressly state in the paragraphs under the title Abstract, that a gap between two adjacent ones of the through holes is smaller than the thickness of the substrate. However, the reference teaches in the paragraph titled CONSTITUTION, that the interval between the through holes is shorter than the wavelength in use. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the gap between the through holes as small for a particular application with an specific frequency, in order to eliminate the cavity resonance phenomena for that particular application.

Regarding claims 5 and 7, the Japanese reference discloses the claimed invention, except for expressly stating in the paragraphs under the title Abstract, that the circuit elements are power-amplifying transistors. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the invention of the Japanese reference (which incidentally is suitable for communication devices due to prevention of cavity resonance phenomena) by implementing power-amplifying transistors as the circuit elements, sine power-amplifying transistors are commonly used in communication devices.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINED